FIG. 1

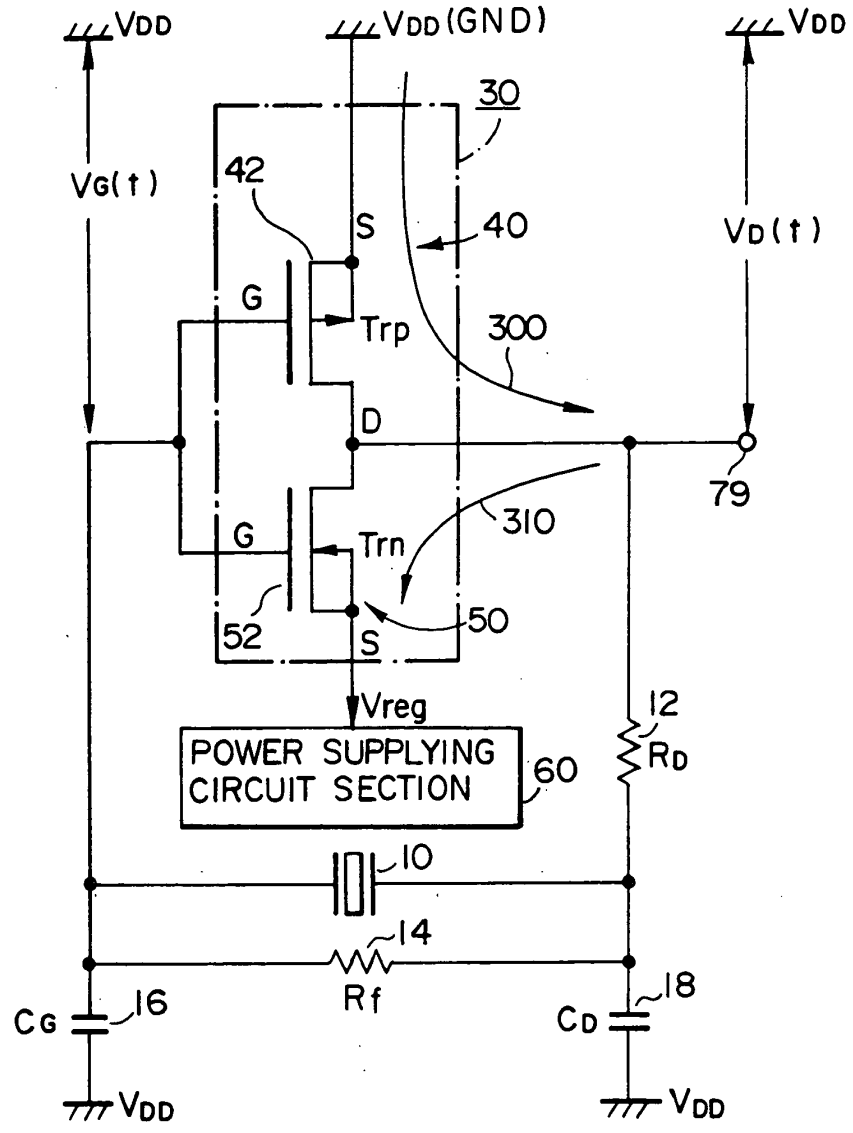

VDD
VDD(GND)
VDD
30
42
S
40
VG(t)
VD(t)
G
Trp
300
D
79
G
Trn
310
52
S
50
Vreg
12
RD
POWER SUPPLYING CIRCUIT SECTION
60
10
14
Rf
CG
16
CD
18
VDD
VDD

FIG. 2
PRIOR ART

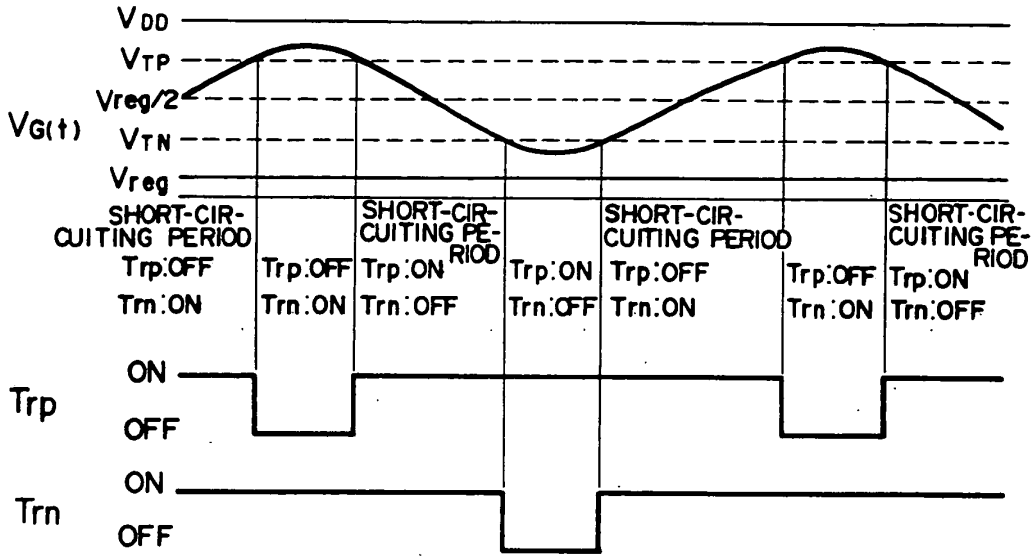


FIG. 3

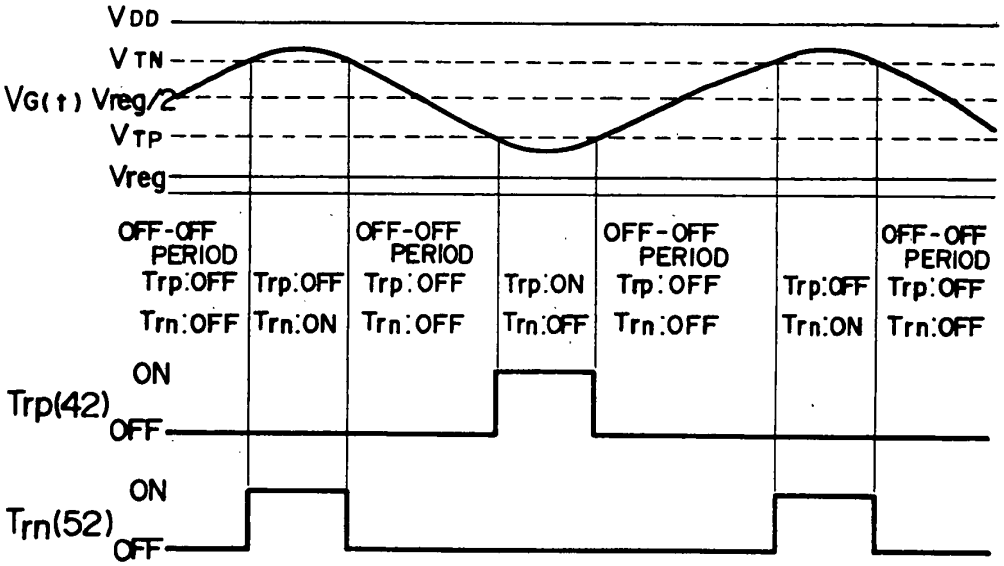


FIG. 4
PRIOR ART

$|V_{reg}| > |V_{TP}| + |V_{TN}|$

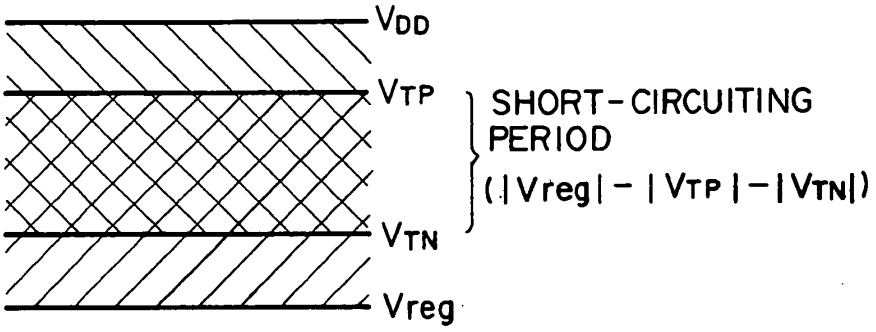


FIG. 5

$|V_{reg}| \leqq |V_{TP}| + |V_{TN}|$

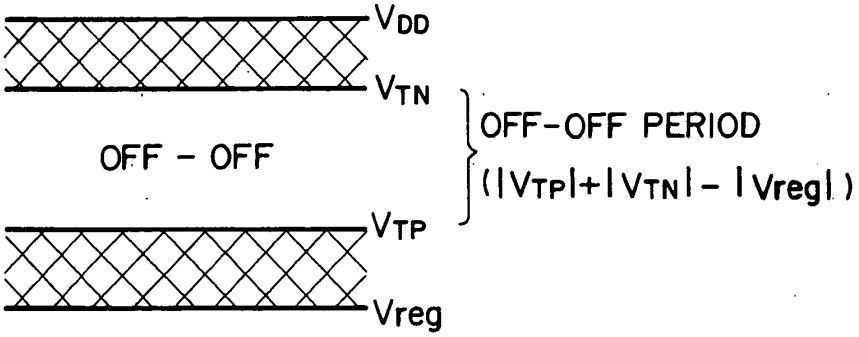


FIG. 6

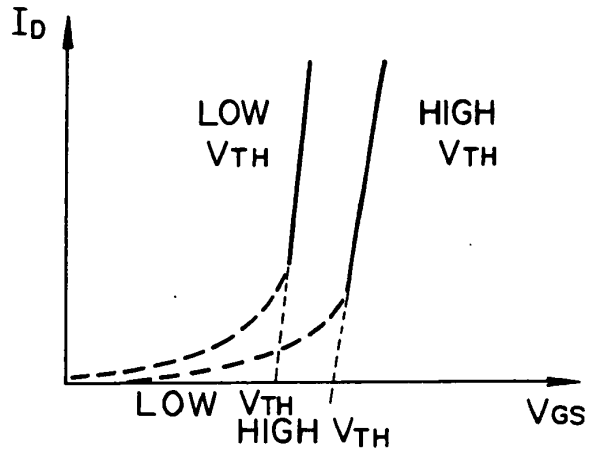

ID
LOW VTH
HIGH VTH
LOW VTH
HIGH VTH
VGS

FIG. 7

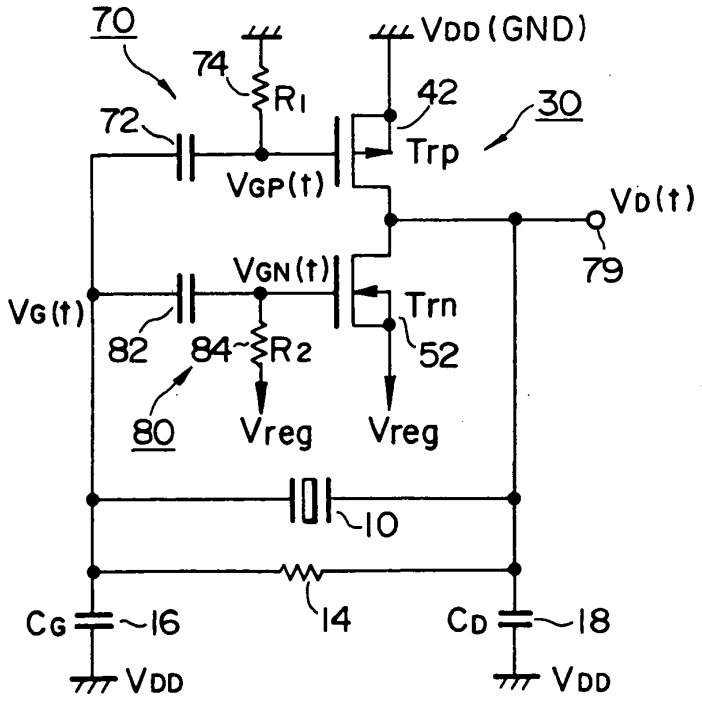
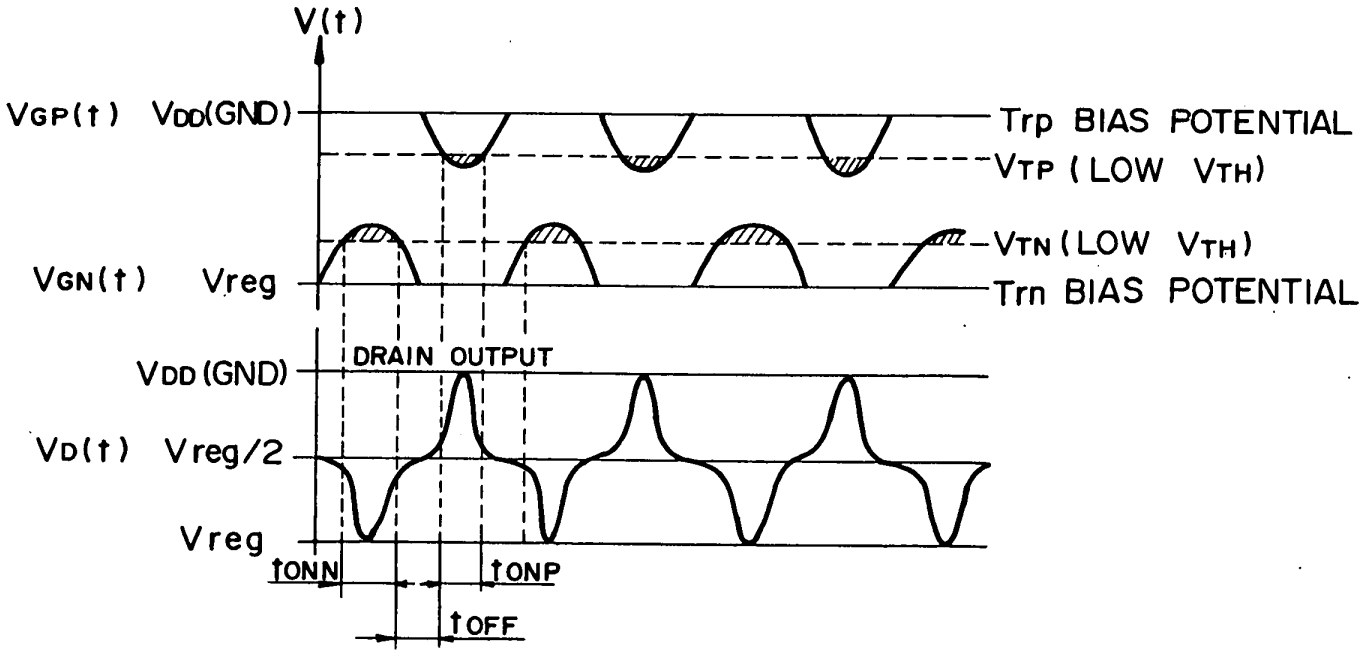

70
74
R1
VDD (GND)
42
30
72
Trp
VGP(t)
VD(t)
79
VGN(t)
VG(t)
Trn
82
84
R2
52
80
Vreg
Vreg
10
14
CG
16
CD
18
VDD
VDD

FIG. 8



t_{ONN} : n-CHANNEL TRANSISTOR ON

t_{ONP} : p-CHANNEL TRANSISTOR ON

t_{OFF} : BOTH OF n-CHANNEL AND p-CHANNEL TRANSISTORS OFF

FIG. 9

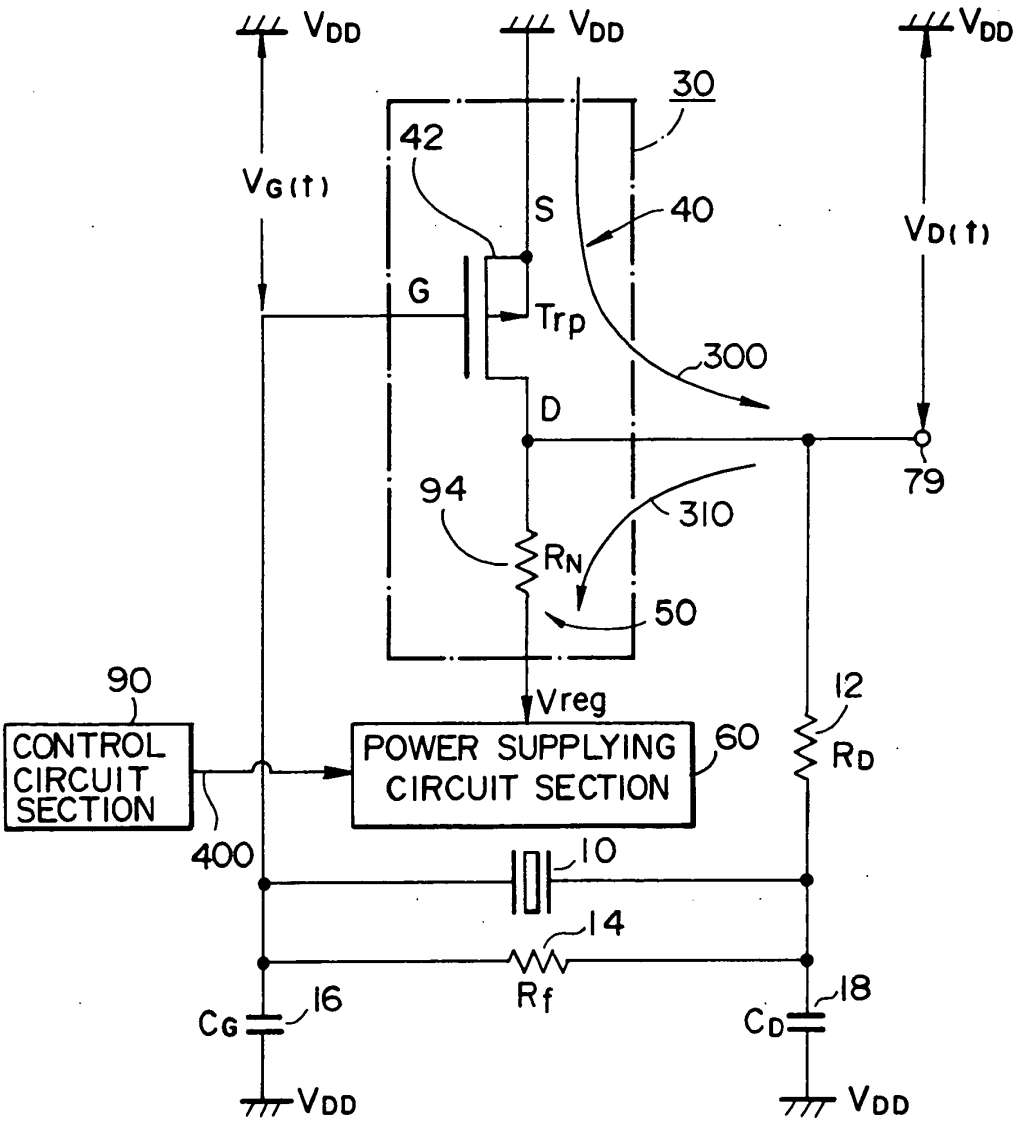

VDD
VDD
VDD
30
42
VG(t)
S
40
VD(t)
G
Trp
300
D
79
94
310
RN
50
90
Vreg
12
CONTROL CIRCUIT SECTION
POWER SUPPLYING CIRCUIT SECTION
60
RD
400
10
14
Rf
16
18
CG
CD
VDD
VDD

FIG. 10

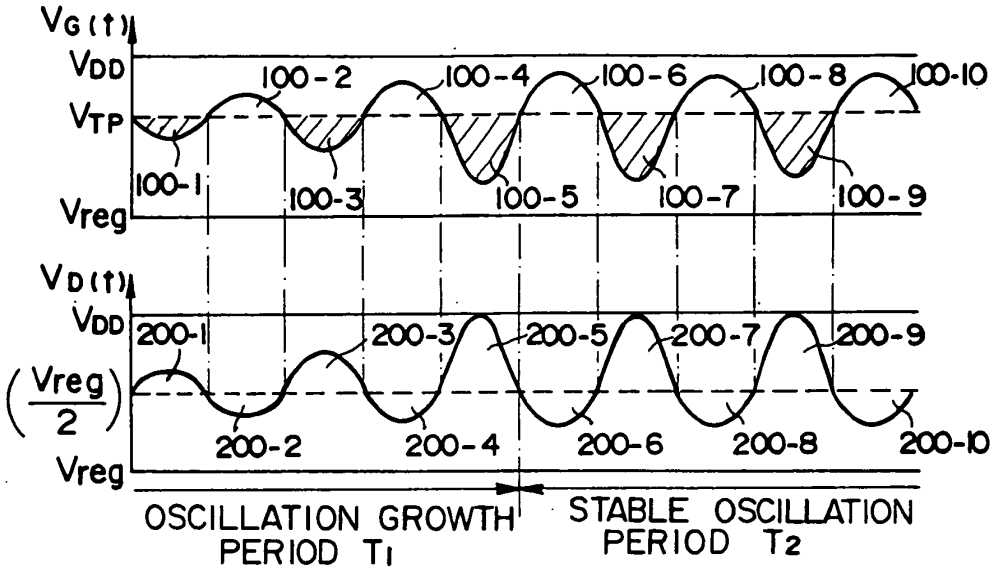

$V_{G(t)}$
V_{DD}
V_{TP}
V_{reg}
100-1
100-2
100-3
100-4
100-5
100-6
100-7
100-8
100-9
100-10
$V_{D(t)}$
V_{DD}
$\left(\frac{V_{reg}}{2}\right)$
V_{reg}
200-1
200-2
200-3
200-4
200-5
200-6
200-7
200-8
200-9
200-10
OSCILLATION GROWTH PERIOD T_1
STABLE OSCILLATION PERIOD T_2

FIG. 11

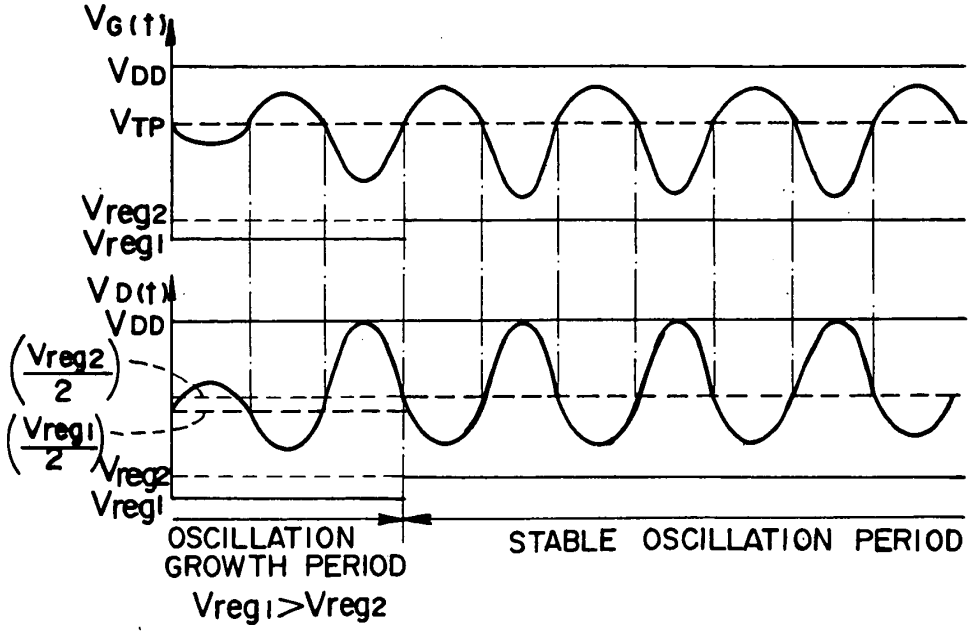

$V_{G(t)}$
V_{DD}
V_{TP}
V_{reg2}
V_{reg1}
$V_{D(t)}$
V_{DD}
$\left(\frac{V_{reg2}}{2}\right)$
$\left(\frac{V_{reg1}}{2}\right)$
V_{reg2}
V_{reg1}
OSCILLATION GROWTH PERIOD
$V_{reg1} > V_{reg2}$
STABLE OSCILLATION PERIOD

FIG. 12

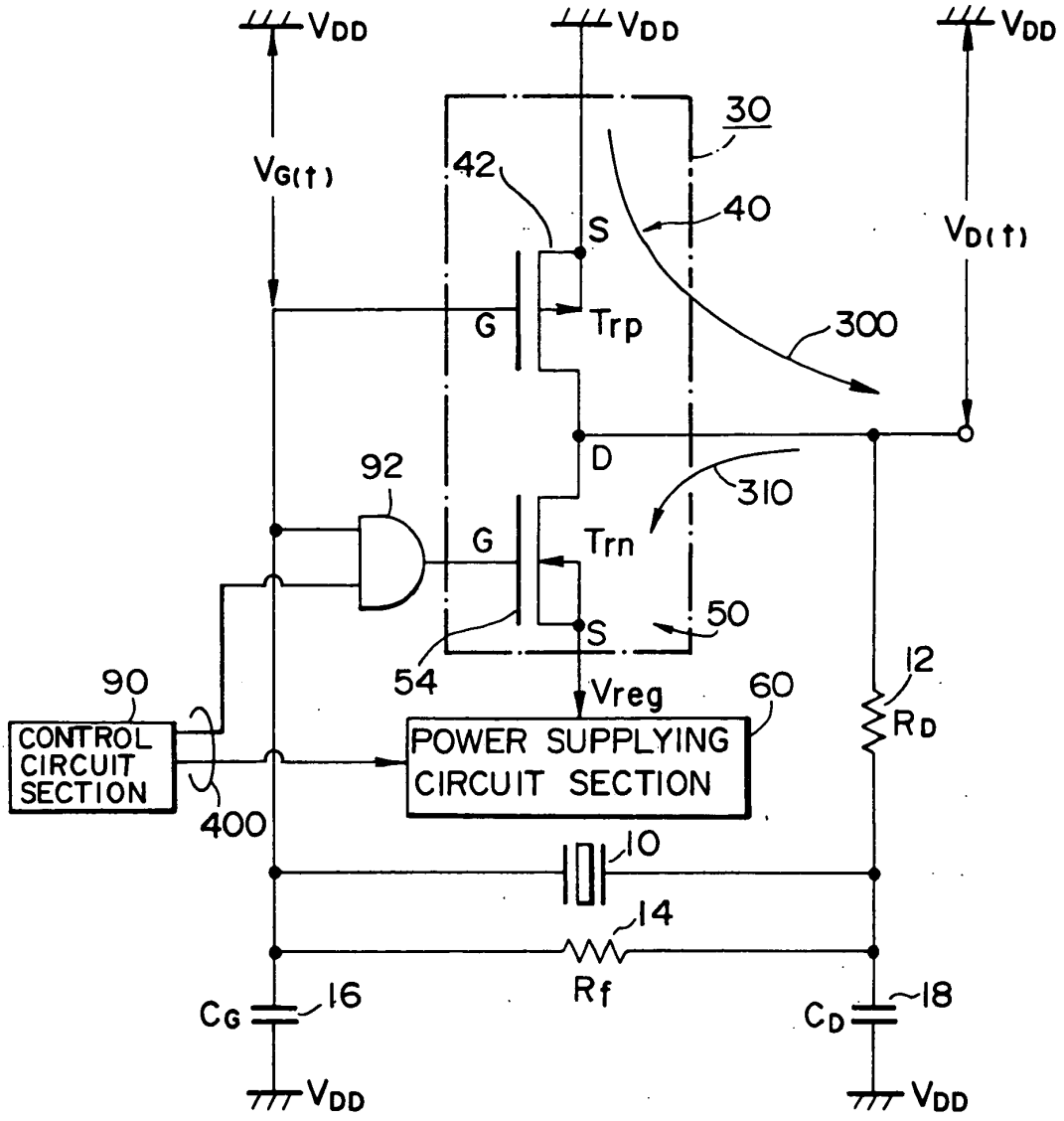

VDD
VDD
VDD
VG(t)
VD(t)
30
42
40
S
G
Trp
300
D
92
310
G
Trn
S
50
54
Vreg
60
12
RD
90
CONTROL CIRCUIT SECTION
400
POWER SUPPLYING CIRCUIT SECTION
10
14
Rf
CG
16
CD
18
VDD
VDD

FIG. 13

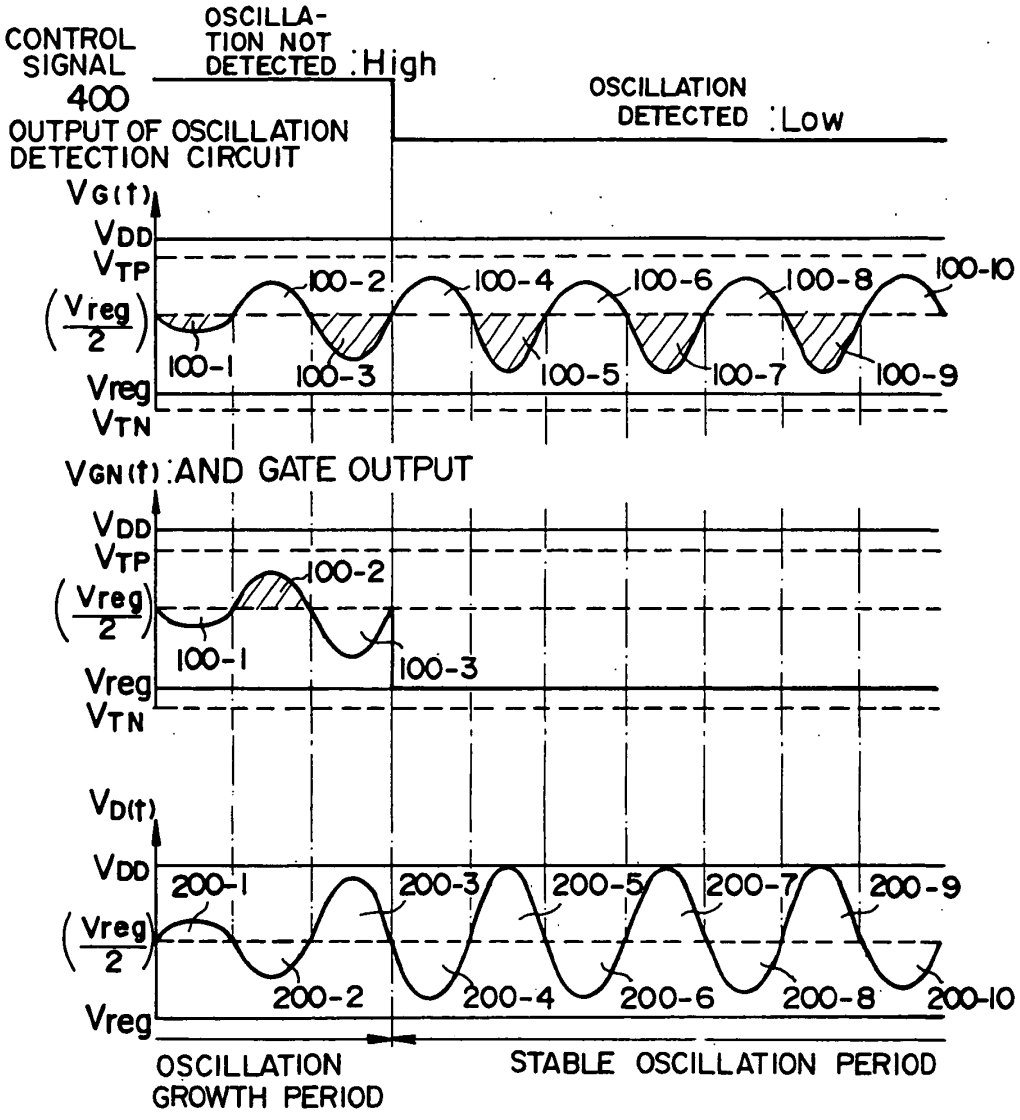

CONTROL SIGNAL
400
OSCILLATION NOT DETECTED : High
OSCILLATION DETECTED : Low
OUTPUT OF OSCILLATION DETECTION CIRCUIT
VG(t)
VDD
VTP
(Vreg/2)
Vreg
VTN
100-1
100-2
100-3
100-4
100-5
100-6
100-7
100-8
100-9
100-10
VGN(t) : AND GATE OUTPUT
VD(t)
200-1
200-2
200-3
200-4
200-5
200-6
200-7
200-8
200-9
200-10
OSCILLATION GROWTH PERIOD
STABLE OSCILLATION PERIOD

FIG. 14

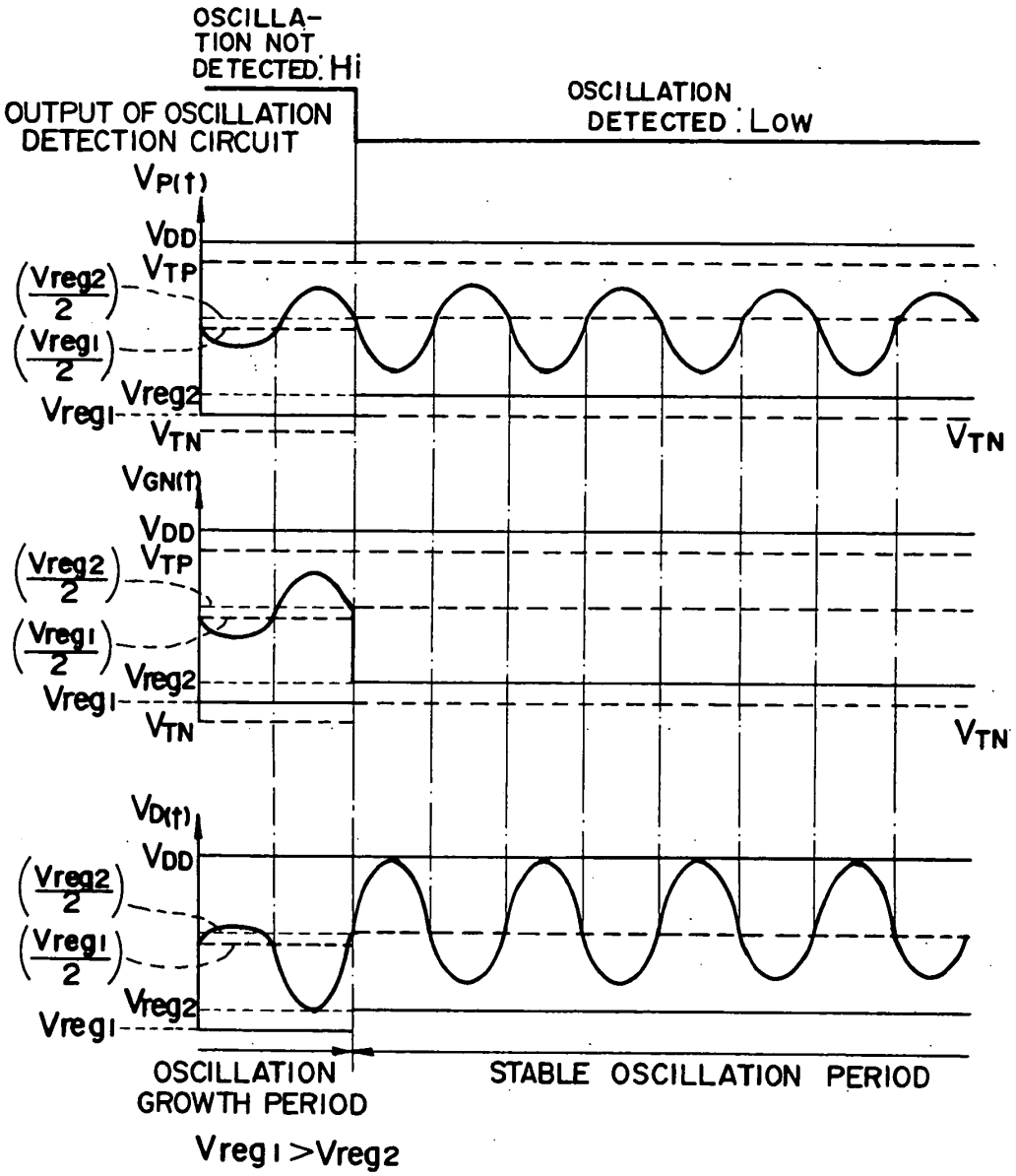

OSCILLATION NOT DETECTED: Hi
OUTPUT OF OSCILLATION DETECTION CIRCUIT
OSCILLATION DETECTED: Low
VP(t)
VDD
VTP
(Vreg2/2)
(Vreg1/2)
Vreg2
Vreg1
VTN
VTN
VGN(t)
VDD
VTP
(Vreg2/2)
(Vreg1/2)
Vreg2
Vreg1
VTN
VTN
VD(t)
VDD
(Vreg2/2)
(Vreg1/2)
Vreg2
Vreg1
OSCILLATION GROWTH PERIOD
STABLE OSCILLATION PERIOD
Vreg1 > Vreg2

FIG. 15

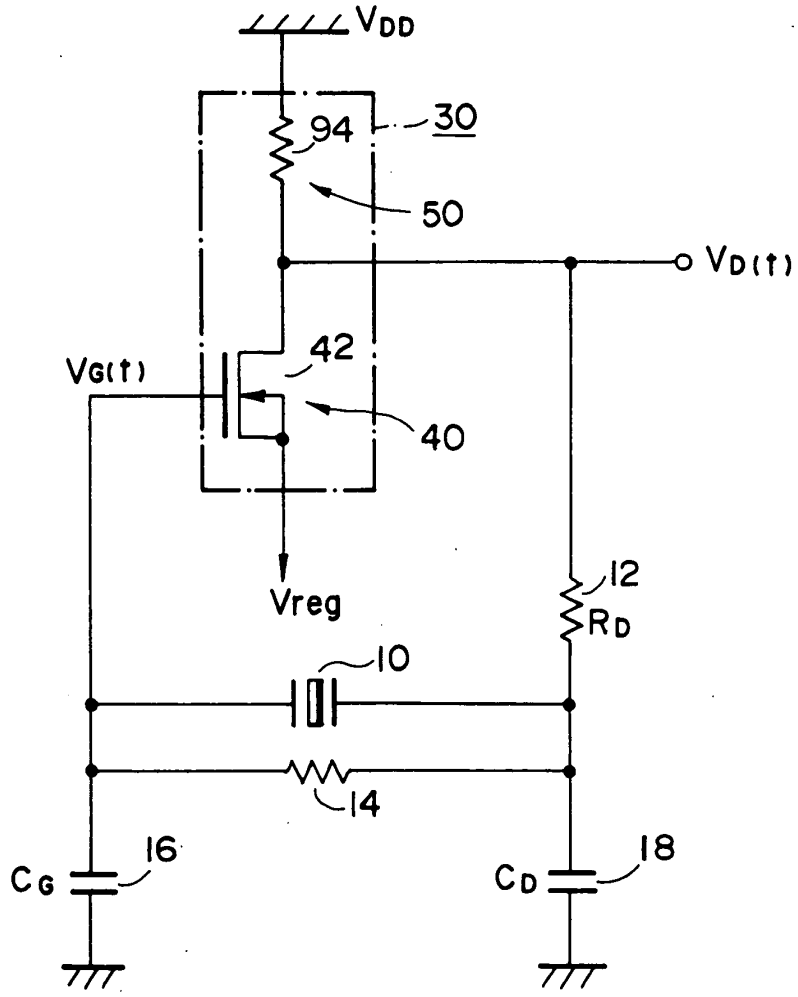


FIG. 16

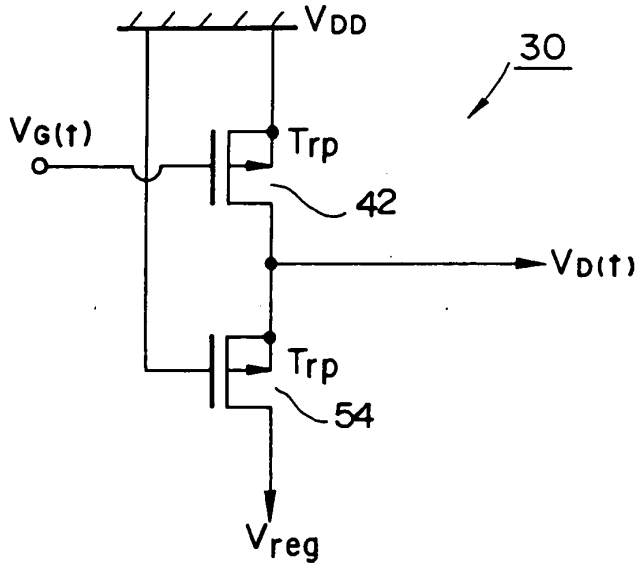

VDD
30
VG(t)
Trp
42
VD(t)
Trp
54
Vreg

FIG. 17

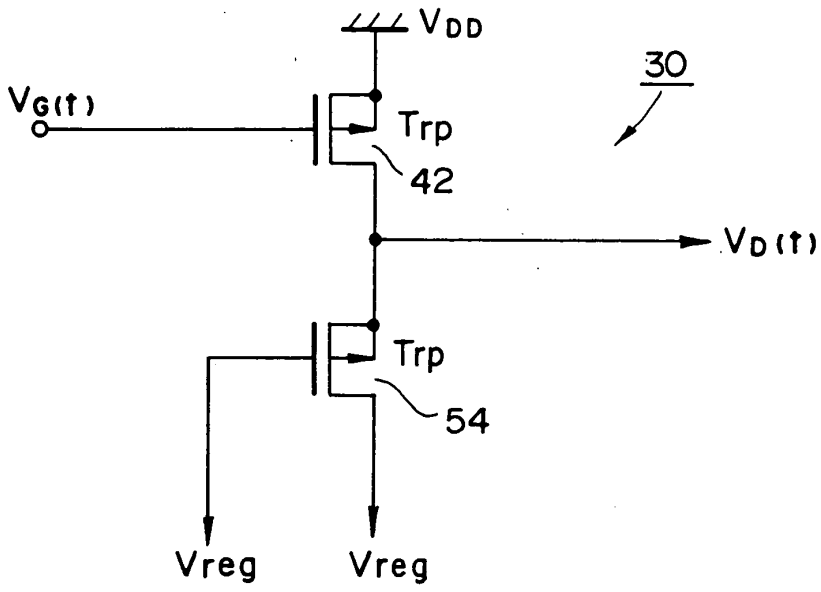

VDD
30
VG(t)
Trp
42
VD(t)
Trp
54
Vreg
Vreg

FIG. 18

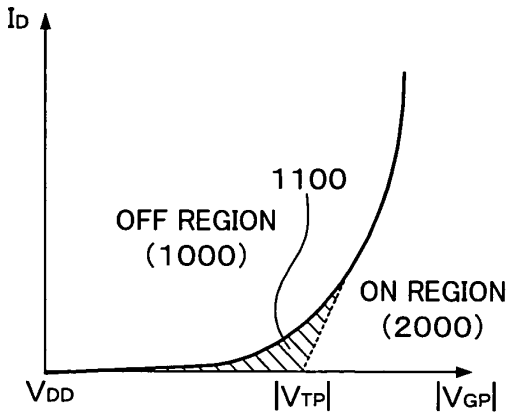

ID
1100
OFF REGION
(1000)
ON REGION
(2000)
VDD
|VTP|
|VGP|

FIG. 19

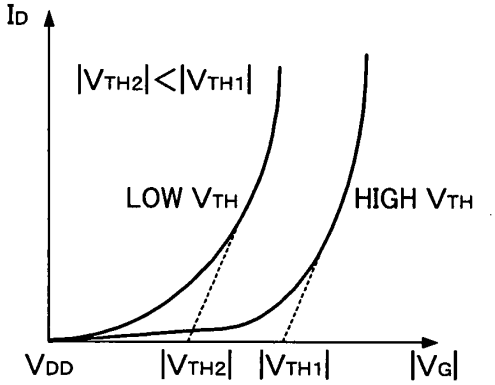

ID
|VTH2|<|VTH1|
LOW VTH
HIGH VTH
VDD
|VTH2|
|VTH1|
|VG|

FIG. 20

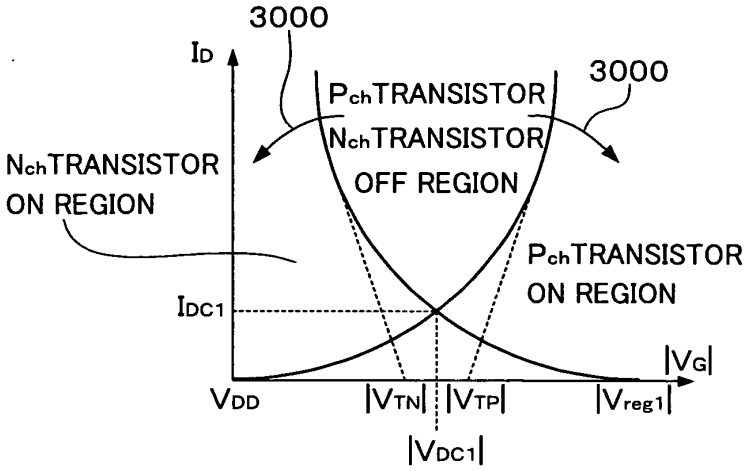

3000
ID
PchTRANSISTOR
NchTRANSISTOR
OFF REGION
3000
NchTRANSISTOR
ON REGION
PchTRANSISTOR
ON REGION
IDC1
|VG|
VDD
|VTN|
|VTP|
|Vreg1|
|VDC1|

FIG. 21

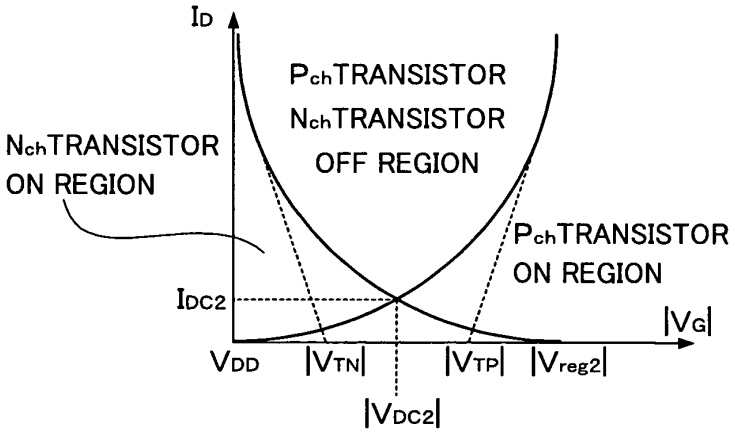

ID
PchTRANSISTOR
NchTRANSISTOR
OFF REGION
NchTRANSISTOR
ON REGION
PchTRANSISTOR
ON REGION
IDC2
|VG|
VDD
|VTN|
|VTP|
|Vreg2|
|VDC2|

FIG. 22

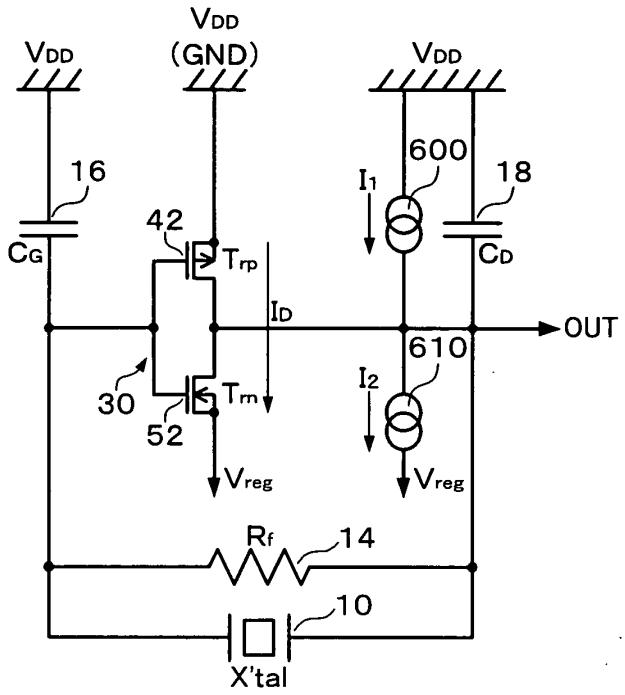

VDD
(GND)
VDD
VDD
16
600
18
I1
42
CG
Trp
CD
ID
OUT
610
30
Trn
I2
52
Vreg
Vreg
Rf
14
10
X'tal

FIG. 23

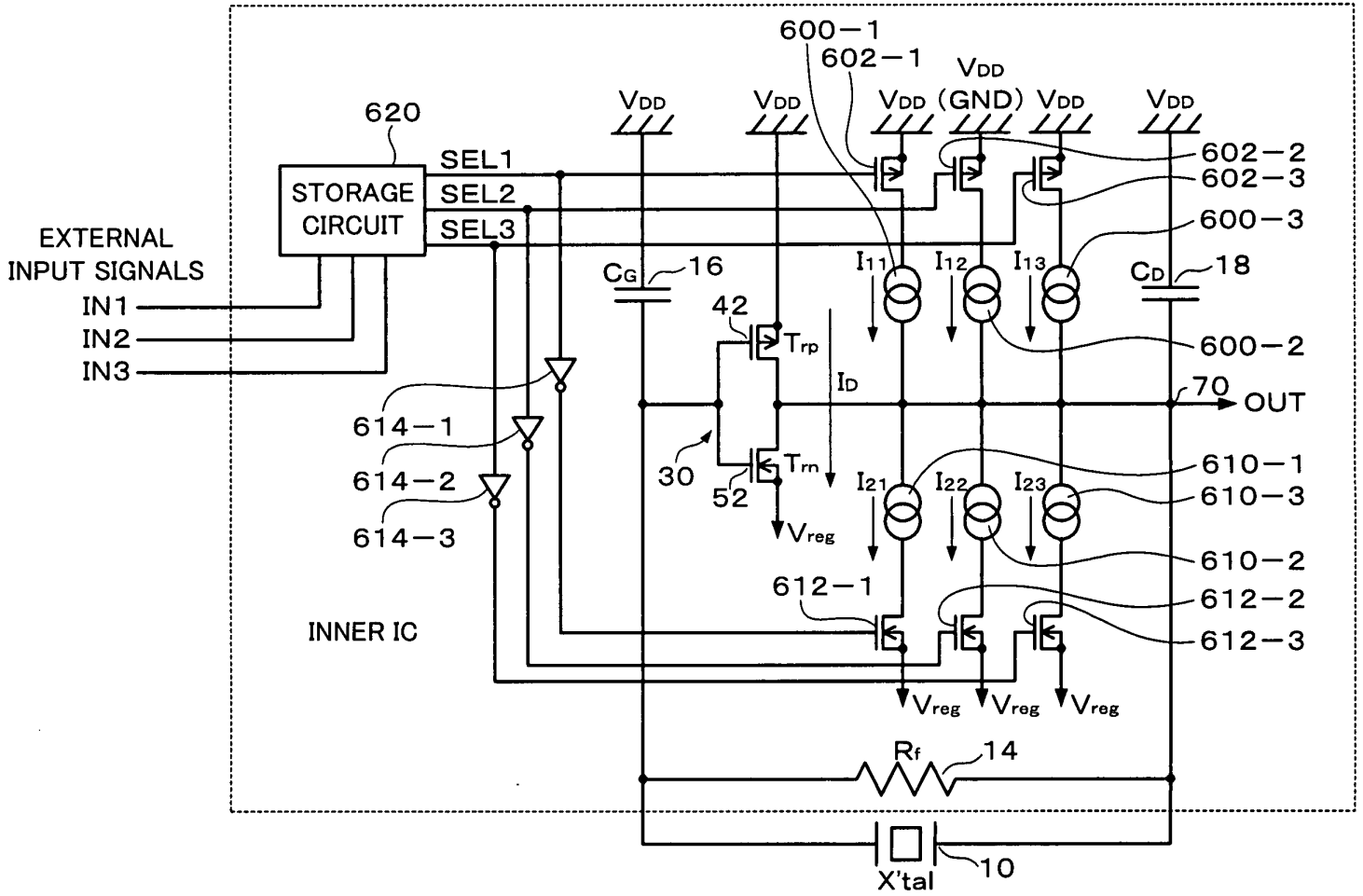
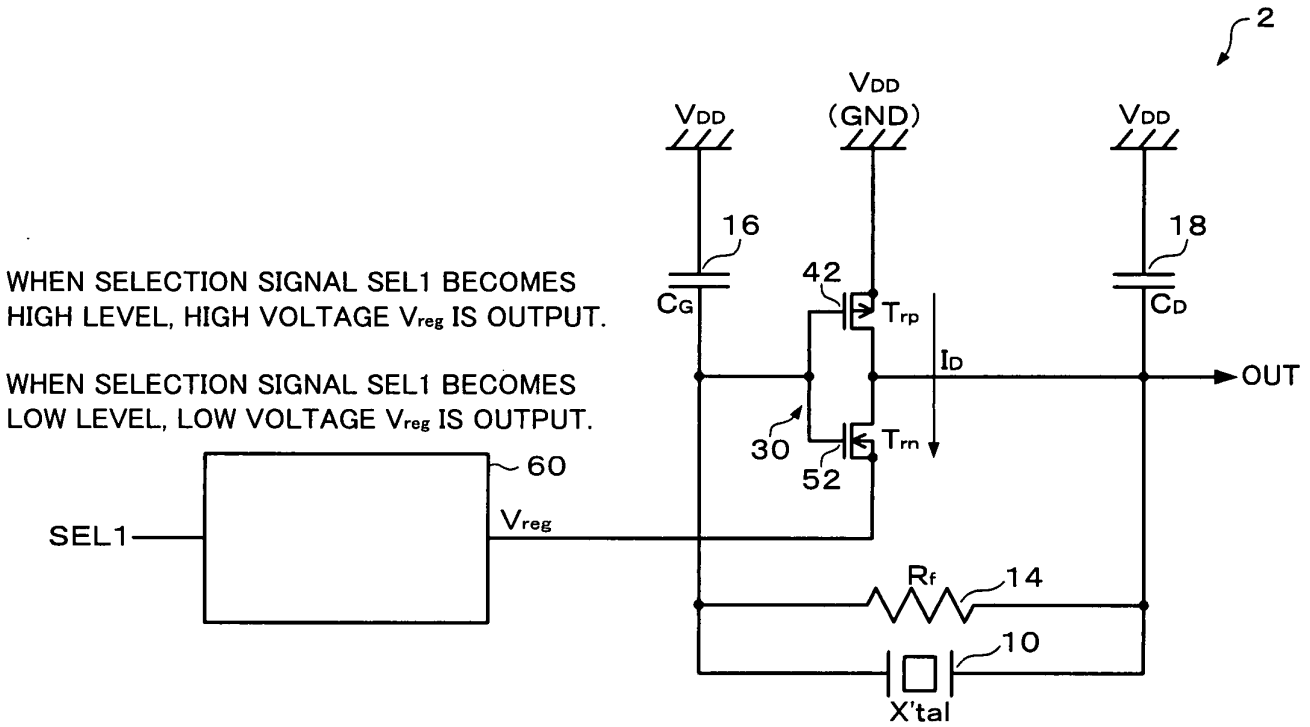

600−1
602−1
VDD
620
VDD
VDD
VDD (GND)
VDD
VDD
602−2
602−3
SEL1
SEL2
SEL3
STORAGE CIRCUIT
600−3
EXTERNAL INPUT SIGNALS
IN1
IN2
IN3
CG
16
I11
I12
I13
CD
18
42
Trp
600−2
ID
70
OUT
614−1
614−2
614−3
30
52
Trn
Vreg
I21
I22
I23
610−1
610−3
610−2
612−1
612−2
612−3
INNER IC
Vreg
Vreg
Vreg
Rf
14
X'tal
10

FIG. 24


2
VDD
VDD
(GND)
VDD
16
18
42
CG
Trp
CD
ID
OUT
WHEN SELECTION SIGNAL SEL1 BECOMES HIGH LEVEL, HIGH VOLTAGE Vreg IS OUTPUT.
WHEN SELECTION SIGNAL SEL1 BECOMES LOW LEVEL, LOW VOLTAGE Vreg IS OUTPUT.
30
52
Trn
60
SEL1
Vreg
Rf
14
10
X'tal

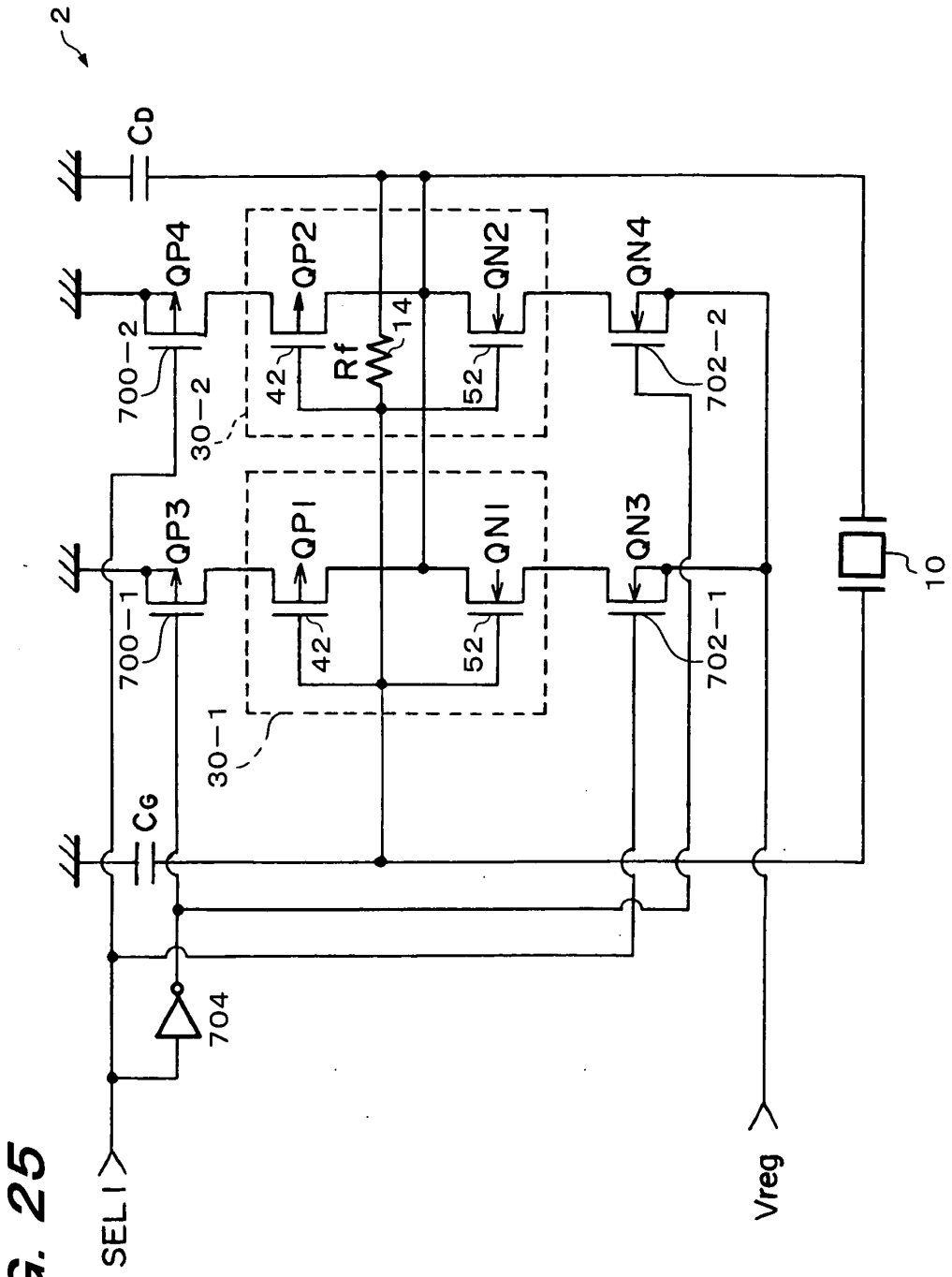

2
CD
QP4
QP2
QN2
QN4
700-2
30-2
42
Rf
14
52
702-2
QP3
QP1
QN1
QN3
700-1
42
52
702-1
10
30-1
CG
704
SEL I
Vreg

FIG. 25

FIG. 26A

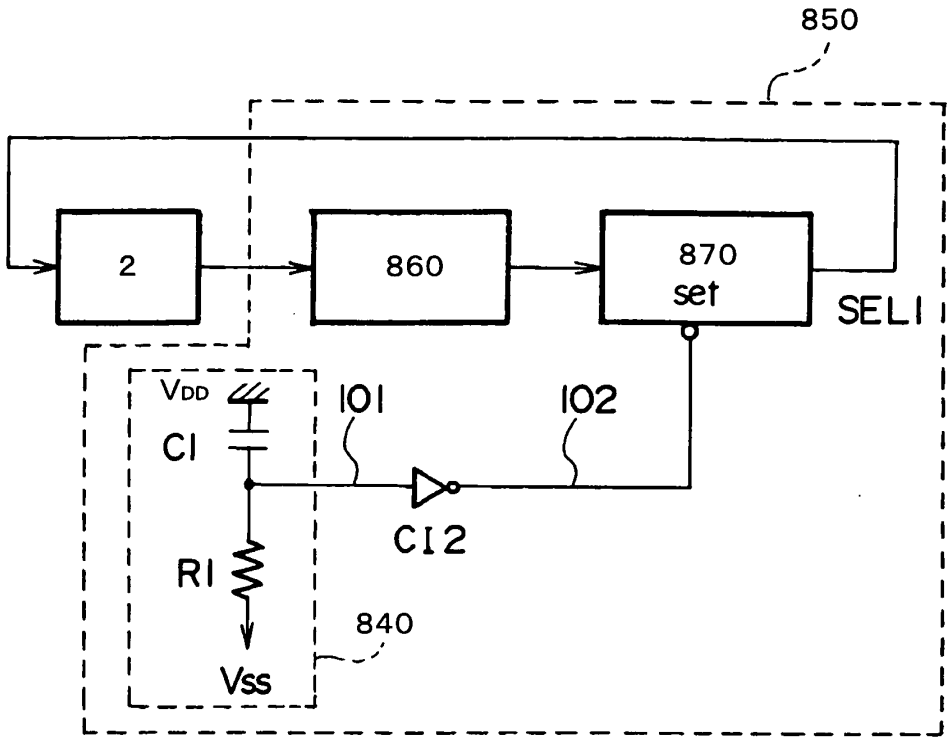


FIG. 26B

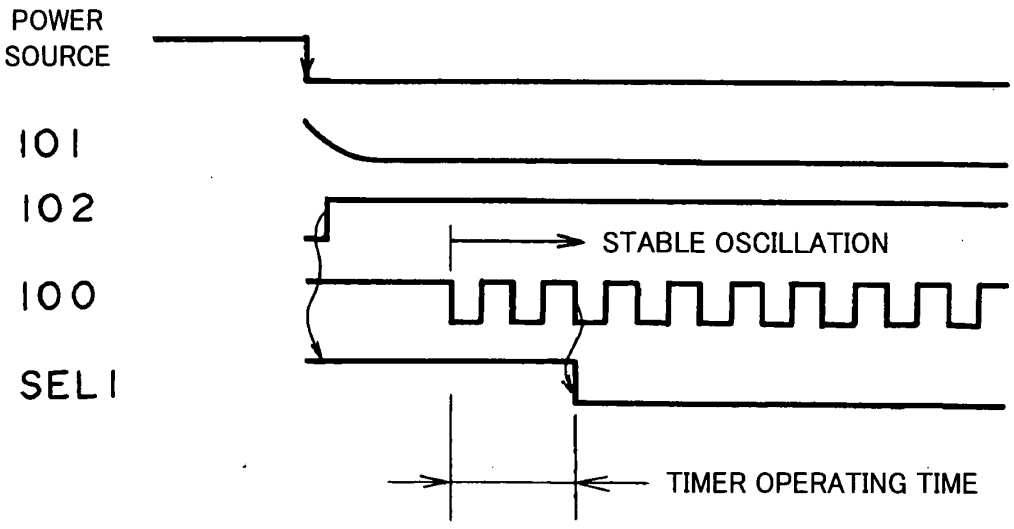


FIG. 27A

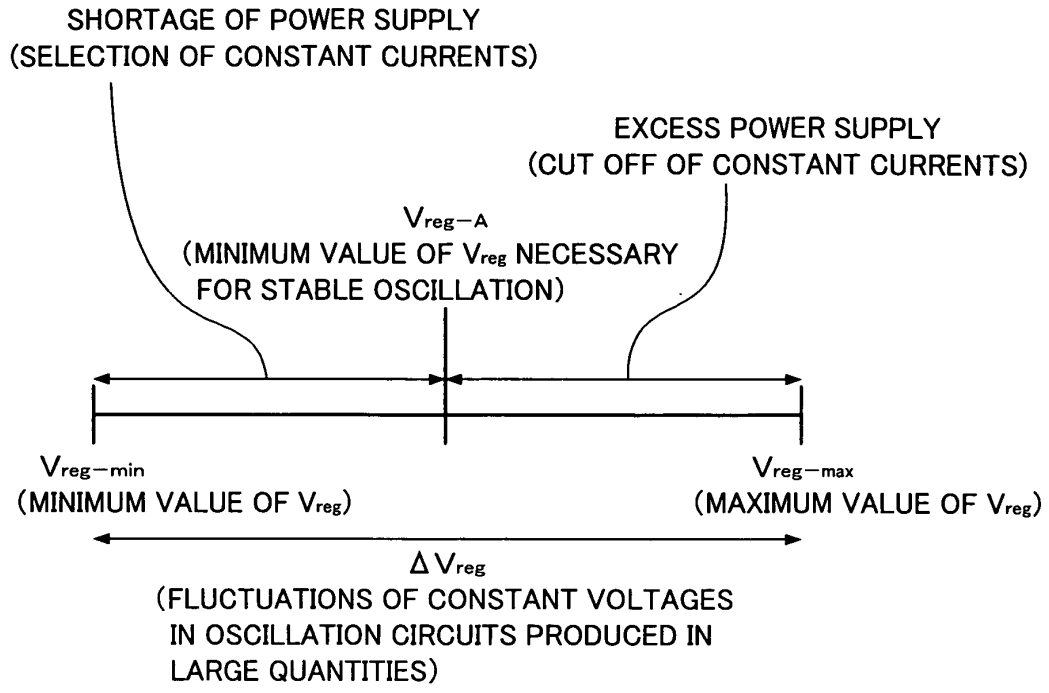


FIG. 27B